## REMARKS

In the office action, claims 1 and 5 were objected to, claims 1 - 8 were rejected

under 35 U.S.C. §112, ¶2 with regard to alleged indefiniteness of claim 1, claims 1 -

4 and 6 - 8 were rejected under 35 U.S.C. §102(b) over U.S. Patent No. 6,015,993 (to

Voldman et al.), claims 1 - 3, 6 - 8 and 13 - 15 were rejected under 35 U.S.C. §102(e)

over U.S. Patent No. 6,344,385 (to Jun et al.), and claim 5 was rejected under 35

U.S.C. §103(a) over Voldman et al. in view of U.S. Patent No. 6,060,752 (to

Williams).

Claims 1 and 5 are amended herein to address the subject matter of the

objections to these claims.

The invention is directed to an electrostatic discharge protective structure that

protects an integrated semiconductor circuit between first and second supply potential

buses of the integrated semiconductor circuit. The electrostatic discharge structure

includes first and second doped regions that are separated by a distance that

corresponds to a dimension of a gate between the first and second doped regions. None

of the cited references, in any combination, teaches, suggests or discloses such a
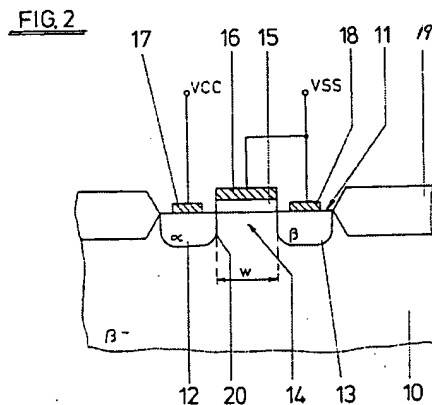
structure.

The Voldman et al. reference discloses a high voltage tolerant diode structure

that includes source and drain diffusion regions 162 and 164 as well as diffusions 142

and 144 between a gate. The gate includes an oxide layer 130, a p-type region 134, an

n-type region 136, a conductive layer 138 and spacers 140. Figure 5 of the Voldman et

al. reference is shown below.
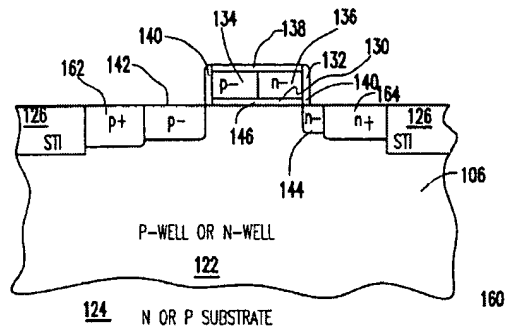
Voldman et al., Figure 5.

The Voldman et al. reference discloses a variety of structures, each of which includes at least one spacer and/or isolation trench between the gate electrode and the doped regions. Although in Figure 5, one side of the gate electrode is aligned with a region 144, the other side of the gate electrode is not aligned with the region 142, but rather is separated therefrom by the spacer 140.

In accordance with applicants' invention as claimed in each of independent claims 1, 13 and 16, the gate electrode 16 has a dimension that corresponds to the distance W between the regions 12, 13 as shown in Figure 2 of the present application, which is reproduced below.

Application, Figure 2.

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The structures of Figure 5, as well as each of the other structures disclosed in the Voldman et al. reference do not include this requirement.

The Jun et al. reference discloses an electrostatic discharge device for integrated circuits that includes a controllable dummy layer diode such as a polysilicon layer to remove shallow trench isolation between n+ and p+ junctions. With reference to Figure 3A thereof, the Jun et al. reference discloses a structure that includes a diode 28 comprised of a p-well or p-substrate 22 as anode and n+ implant 13 as cathode, and has a controllable dummy polysilicon layer 35 disposed as a clamp device between gate 33 and a source 32 of a MOS type semiconductor device for MOS protection. Jun et al., col.3, lines 13 - 18.
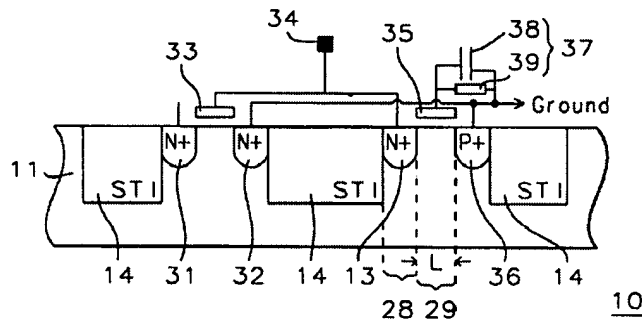
Jun et al., Figure 3A.

The devices of Jun et al. do not include two doped regions separated by a distance that corresponds to the dimension of a gate electrode therebetween as required by each of claims, 1, 13 and 16.

The Williams reference discloses an electrostatic discharge protection circuit that includes diodes connected in series between the signal input and power supply terminals of the circuit to be protected. The William reference, however, also does not

disclose a circuit that includes two doped regions separated by a distance that corresponds to the dimension of a gate electrode therebetween as required by each of claims, 1, 13 and 16.

In particular, independent claim 1 as amended requires in part, a gate electrode that is located between first and second regions with the first region being separated from the second region by a distance that corresponds to a dimension of the gate electrode. Independent claim 13 as amended similarly requires in part, a gate electrode having a width W and being located between first and second regions such that the first and second regions are separated by the width W. New independent claim 16 requires in part, an insulator located between first and second electrodes of first and second regions, and having a dimension that corresponds to the distance between the first and second regions, and a gate electrode in communication with and contiguous with the insulator.

None of the references in any combination, discloses, teaches or suggests such structures as claimed in claims 1, 13 or 16. Each of claims 1, 13 and 16, is therefore submitted to be in condition for allowance for at least this reason. Each of dependent claims 2 - 8 depends from claim 1 and further limits the subject matter thereof. Each of dependent claims 14 and 15 depends from claim 13 and further limits the subject matter thereof, and each of claims 17 and 18 depends from claim 16 and further limits the subject matter thereof. Each of claims 1 - 8 and 13 - 18 is considered to be in condition for allowance.

Moreover, independent claim 16, as well as dependent claims 14, 17 and 18,

each further require an insulator (claim 16) or a gate oxide (claims 14, 17 and 18) that is in contact with the gate electrode. None of the references of record further include this feature. The structures of Voldman et al. include semiconductor material in the gate, the devices of Jun et al. include no such disclosure of an insulator such as an oxide, and the circuits of Williams also include no disclosure of an insulator such as an oxide that underlies a gate electrode having a dimension that corresponds to the distance between two adjacent doped regions.

Applicants respectfully submit that each of claims 1 - 8 and 13 - 15 as well as each of new claims 16 - 18 is in condition for allowance. Favorable action consistent with the above is respectfully requested.

Respectfully submitted,

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